



SARDAR PATEL INSTITUTE OF TECHNOLOGY
Munshi Nagar, Andheri (W) Mumbai 400 058
(Affiliated to University of Mumbai)

Centre: 735, SPIT

Office register for T.E., Electronics Engineering, Semester V (CBGS), Exam: First Half December 2020 (A.T.K.T)

Courses →		EXC501			EXC502			EXC503			EXC504				EXC505			EXS506				EXL501			EXL502			EXL503			EXL504			TOTAL	SGPI (GPA)	RESULT
		Microcontrollers and Applications			Design with Linear Integrated Circuits			Electromagnetic Engineering			Signals and Systems				Digital Communication			Business Communication and Ethics				Microcontrollers and Applications Laboratory			Design with Linear Integrated Circuits Laboratory			Digital Communication Laboratory			Mini Project I					
Seat No / Name of Student ↓		ESE	IA	TOT	ESE	IA	TOT	ESE	IA	TOT	ESE	IA	TOT	TW	ESE	IA	TOT	TW				PR OR	TW	TOT	PR OR	TW	TOT	OR	TW	TOT	OR	TW	TOT			
	MaxM	80	20	100	80	20	100	80	20	100	80	20	100	25	80	20	100	50				25	25	50	25	25	50	25	25	50	25	25	50	775		
	MinM	32	8	40	32	8	40	32	8	40	32	8	40	10	32	8	40	20				10	10	20	10	10	20	10	10	20	10	10	20			
35101	MarksO	61	18+	79	47+	16+	63	67	15+	82	38+	11+	49	15+	38+	09+	47	23+				10+	11+	21	14+	10+	24	12+	11+	23	11+	10+	21	447	6.54	P
SHAH KARAN RAKESH JAGRUTI	Grade	A	O	A	D	O	C	O	A	O	E	D	E	C	E	E	E	E				P	P	P	D	P	E	E	P	E	P	P	P			
	C			4			4			4			4	1			4	2						1			1			1			2	28		
	GP*C			36			28			40			20	7			20	10						4			5			5			8	183		

Female	/
0.229	#
0.5042	@
0.5045	*
3.4CBGSM	!
0.5050	RCC
Pass	P
Fail	F
Exempted	E
Reserved for Lower Exam	RLE
Dyslexia Benefit	~

Credit	C
Grade	G
Grade Point	GP
C*GP	CGP
Sum of Credits	ΣC
Sum of CGPs	ΣCGP
ΣCGP/ΣC	GPA
Null & Void	NULL
Absent	Ab

% Marks	Grade	GP
M>=80	O	10
75>=M<80	A	9
70>=M<75	B	8
60>=M<70	C	7
50>=M<60	D	6
45>=M<50	E	5
40>=M<45	P	4
M<40	F	0

Entered by

Checked by

Verified By

Principal



Principal
Sardar Patel Institute of Technology
Bhavan's Campus,
Munshi Nagar, Andheri (West)
Mumbai - 400 058