SARDAR PATEL INSTITUTE OF TECHNOLOGY

Munshi Nagar,Andheri (W) Mumbai 400 058

(Affiliated to University of Mumbai)

Centre: 735, SPIT

Office register for S.E., Electronics Engineering, Semester III (CBGS), Exam: First Half December 2020 (A.T.K.T)

Courses →		EXS301 Applied Mathematics – III				EXC302 Electronic Devices			EXC303 Digital Circuits and Design			EXC304 Circuit Theory			EXC305 Electronic Instruments and Measurements			EXL301 Electronic Devices Laboratory			EXL302 Digital Circuits and Design Laboratory			EXL303 Circuit Theory and Measurements Laboratory	EXL304 Object Oriented Programming Methodology Laboratory			TOTAL	SGPI (GPA)	RESULT
Seat No / Name of Student ↓		ESE	IA	TOT	TW	ESE	IA	TOT	ESE	IA	TOT	ESE	IA	TOT	ESE	IA	TOT	PR OR	TW	TOT	PR OR	TW	TOT	TW	PR OR	TW	TOT			
	MaxM	80	20	100	25	80	20	100	80	20	100	80	20	100	80	20	100	50	25	75	50	25	75	25	50	25	75	775		
	MinM	32	8	40	10	32	8	40	32	8	40	32	8	40	32	8	40	20	10	30	20	10	30	10	20	10	30			
23101	MarksO	54	08+	62	12+	35+	11+	46	32+	10+	42	41+	14+	55	32+	11+	43	33+	20+	53	42+	19+	61	20+	39+	19+	58	452		
	Grade	C	P	C	E	P	D	E	P	D	P	D	B	D	P	D	P	C	O	B	O	A	O	O	A	A	A			
GITE PRASAD SHRIPAD SANGITA	C			4	1			4			4			4			4			1			1	01			02	26		
	GP*C			28	5			20			16			24			16			8			10	10			18	155	5.96	P

Female	/
0.229	#
0.5042	@
0.5045	*
3.4CBGSM	!
0.5050	RCC
Pass	P
Fail	F
Exempted	E
Reserved for Lower Exam	RLE
Dyslexia Benefit	~

Credit	C
Grade	G
Grade Point	GP
C*GP	CGP
Sum of Credits	∑C
Sum of CGPs	∑CGP
∑CGP/∑C	GPA
Null & Void	NULL
Absent	Ab

% Marks	Grade	GP
M>=80	O	10
75>=M<80	A	9
70>=M<75	B	8
60>=M<70	C	7
50>=M<60	D	6
45>=M<50	E	5
40>=M<45	P	4
M<40	F	0

Entered by Checked by Verified By Principal

Principal
Sardar Patel Institute of Technology
Bhavan's Campus,
Munshi Nagar, Andheri (West)
Mumbai 400 058