Two Day

Faculty Development Programme (FDP)

on

"Laboratory Experimentation with Cadence Toolset for Analog VLSI Design"

14th- 15thDec 2016

To,

Department of ElectronicsEngineering,
Sardar Patel Institute of Technology,
Munshi Nagar, Andheri (W),
Mumbai 400 058
Phone: 26707440/26708520 Extn. 350

From,

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Patrons:
Dr. Prachi Gharpure, Principal
Dr. Y.S. Rao, Vice-Principal

Coordinator and Contact for Registration:
Dr. Surendra Rathod
Phone: 26707440/26708520Extn. 350
Mobile:9920228275
Email:surendra_rathod@spit.ac.in

Email for communication:
fdp@spit.ac.in

Registration:
Please fill online registration at
http://www.spit.ac.in/2016/11/29/two-day-fdp-on-laboratory-experimentation/

Resource Persons:
Mr.Venugopal D Kulkarni
(Consultant - Analog/ Mixed Signal Circuits and Systems Design)
Mr.Binu Alias (VLSI Application Engineer)

How to Reach:
1. By Air: Santacruz Airport (5 Km)
2. By Train: Andheri Station (1.5 Km)
3. By Metro: Azadnagar Station (0.5 Km)
4. By Bus From Andheri (W) station:249/250/254/257/259

Venue: Sardar Patel Institute of Technology
Bhavan's Campus, Munshi Nagar,
Andheri (W),Mumbai 400 058
Tel: 91-22-2670 8520, 26707440, 2628 7250
Fax No.: 91-22-26701422

BharatiyaVidyaBhavan's
Sardar Patel Instituteof Technology

Announces

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Organized by

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Tel: 91-22-2670 8520, 26707440, 2628 7250
Fax No.: 91-22-26701422
www.spit.ac.in

About us

Sardar Patel Institute of Technology is under the umbrella of Bharatiya Vidya Bhavan & is academically affiliated to the University of Mumbai. Institute runs four UG , three PG and two Ph.D. programmes. Department of Electronics Engineering has earned a great reputation in the field of engineering education, as well as industry.The department has well equipped laboratories to cater the curriculum. The department regularly organizes value added courses and STTPs. Department is provisionally accredited by National Board of Accreditation.

About the FDP

Integrated circuits incorporating both digital and analog functions have become increasingly prevalent in the semiconductor industry. Complex digital circuits are now commonly combined with analog circuits as part of the continuing drive toward higher levels of electronic system integration. Apart from difficult task of optimization, one has to consider various nonidealities introduced by devices. Analog circuit design is therefore challenging task. Now necessity of analog circuit designers is being acutely felt by electronic industry.
This course is primarily on the cadence toolset. Teachers from Mumbai University who conduct experiments for CMOS Analog VLSI Design will be useful.

Registration Fee:

Registration charges of Rs. 800/--in the form of Demand Draft/Cheque in favor of "Principal, Sardar Patel Institute of Technology" payable at Mumbai should reach to us on or before 10th Dec 2016 along with registration form. **Charges will not be returned if candidate is selected and does not attend the course**.

Selection Criteria:

Maximum 30 participants on **'First Come First Serve Basis'**. Organizing committee's decision will be final in selecting the participants.

Course Contents/Highlights:

Day 1: Fundamentals of Analog Signal Processing – CMOS Amplifier Topologies and Performance

- Review of the generic amplifier performance parameters – Gain, Power Dissipation, Frequency Response, (Noise – optional, time permitting)

·Synthesis of Basic Amplifier Circuit Topologies

o Basic Amplifier Circuit Topologies: CS, CD and CG

· Large and Small Signal DC Performance Analysis and Design of Basic Amplifiers

Single and Differential Ended Signaling – Concept Illustration - What really is a common mode signal?

· The Basic Ideal OP-AMP and its properties

o What really is *virtual short* and *virtual ground*?

- Lab1: PDK Device Characterization for Analog Model Parameters
- Lab 2: Hands – on Tutorial on Design and Simulation of a CS Amplifier for Large and Small Signal DC performance
- Lab 3: Design and Simulation of the Bias Circuit for the CS amplifier: Hands – on Tutorial

Day 2: Small Signal DC Design and Simulation of the Basic Differential Pair/ Analog Layout Design Concepts

- Interpreting the Design Specifications

· Design Methodology and Flow - Large Signal and Small Signal DC Design

· Analog Layout Design Concepts – Importance of Device Matching in Layouts; LDEs

· Lab 4: Design and Performance Characterization of CMOS Current Mirror (Schematic Design and Simulation)

· Lab 5: Layout Design of a CMOS Current Mirror

· Lab 6: DC Performance Characterization of the Basic CMOS Differential Amplifier

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Name: _____

Designation: _____

Qualification: _____

Institution:_____

Address: _____

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Email: _____

Tel: (O) _____(Extn.) _____

(M)_____(R)_____

Payment by DD/Cheque drawn in the favor of "Principal, Sardar Patel Institute of Technology", payable at Mumbai of Rs. 800/--:

DD No: _____ **Dated:**_____

Bank: _____

Signature of the participant