Patrons:
Dr. Prachi Gharpure, Principal
Dr. Y.S. Rao, Vice-Principal

Coordinator:
Dr. Surendra Rathod
Professor and Head, Electronics Engineering Dept.
Phone: 26707440/26708520 Extn. 350
Mobile: 9920228275
Email: surendra_rathod@spit.ac.in

Course Fees: Rs. 1,500/-

Total Seats: 20. Selection will be done on 'First Come First Serve Basis'.

Registration:
Cheque or Cash or DD drawn in the name of **"SPIT, Allied division"** payable at Mumbai should reach on or before 30th Mar 2016 along with the online registration.
For online registration please visit
http://www.spit.ac.in/2016/03/04/iste-approved-one-week-sttp-on-outcome-based-education-innovative-teaching-learning-practices-and-evaluation/

Please note that registration charges are ***non-refundable*** *under any circumstances.*

Contact:
Prof. Payal Shah (Mobile: 9867368965)
Email: payal_shah@spit.ac.in

Important Dates:
Last Date for Registration/DD: 15th Apr 2016
Notification of Selection: 20th Apr 2016

Venue: Room No: 008, Ground Floor, S.P.I.T. Bhavan's campus, Munshi Nagar, Andheri (W), Mumbai: 400 058

About us

Electronics Engineering Department, since its inception in 1995, has achieved great recognition in the field of technical education. The department offer B.E. in Electronics Engineering, a four-year degree program with an intake of 60 students. The department has well equipped laboratories to cater the curriculum. It comprises qualified and professionally skilled faculty members with an impressive record of the published work. Department faculties are rigorously involved in R&D activities. Their research work is published in reputed international journals like IEEE, IET, AIP, ASP, Elsevier, Wiley, IETE etc. and also in international conferences. The faculty members conduct training programs in the various areas of engineering such as embedded systems, VLSI and networking. The National Board of Accreditation accredited the department in 2004 and 2013.

At Sardar Patel Institute of Technology, we have adopted several innovative teaching learning practices and evaluation mechanisms. These pedagogy methods are appreciated by several stakeholders and educationist across the country. There are faculty members in the institute who are regularly called as resource persons for conducting workshops on outcome based education and also as auditors/members of advisory boards etc.

Organizing Committee:
1. Prof. Narendra Bhagat
2. Prof. Payal Shah
3. Prof. Manisha Bansode
4. Prof. Shailesh Rokade
5. Prof. Vijaylaxmi Bhat
6. Prof. Manoj Gofane

Bharatiya Vidya Bhavan's
Sardar Patel Institute of Technology

Announces

ISTE Approved One week STTP on

Outcome Based Education-Innovative Teaching Learning Practices and Evaluation

(02nd May to 06th May, 2016)

Organized by

Department of Electronics Engineering,
Sardar Patel Institute of Technology,
Munshi Nagar, Andheri (W),
Mumbai 400 058
Tel: 91-22-2670 8520, 26707440, 2628 7250
Fax No.: 91-22-26701422
www.spit.ac.in

About the Workshop

NBA (National Board of Accreditation) has introduced a new process, parameters and criteria for accreditation. These are in line with the best international practices and oriented to assess the outcomes of the programme. Accreditation is a process of quality assurance and improvement, whereby a program in an approved Institution is critically appraised to verify that the program continues to meet and/or exceed the Norms and Standards prescribed by regulator from time to time. It is a kind of recognition which indicates that a program fulfills desired standards.

For accreditation, institute need to follow certain processes for improving the quality of education. The teachers need to understand and then implement the various processes required to improve the quality of teaching learning. This workshop primarily is designed to provide platform to the teachers of engineering colleges to understand the various processes of teaching learning and participate in the innovations.

Articulation of course outcomes, programme outcomes, their assessment and evaluation is still not clearly understood by many teachers. Articulation of course outcomes for a particular course, various direct and indirect assessment techniques and their evaluation will be covered in detail in this course. Best practices followed for teaching learning at Sardar Patel Institute of Technology will be discussed in this workshop. Organizers also wish that through this collaborative learning sharing of the knowledge of processes followed at other institutions will help participants as well as host institution in imparting the quality education.

Advancements in communication technologies have significantly affected teaching learning processes. People are taking about the virtual universities. Worldwide concept of self learning is gaining importance day by day. Self learning can be done through remote laboratory i.e. the use of communication technology to perform real experiments at the physical location of the operating technology, whilst the teacher/student is utilizing technology from a separate geographical location. The benefit of learning on your own is that you can explore different ways of thinking, and you can go through difficult concepts on your own without help. It enhances the sharing of knowledge, expertise and resources. It improves the learning outcomes of a student. Through this workshop we will provide hands on training to the participants on self learning strategies in the areas of FPGA programming and Embedded Systems.

Assessment and evaluation of various laboratory experiments consumes significant time of an instructor. Now traditional methods of content delivery and assessment are to be supported with innovative assessment methods. It requires the smart tools which will accurately do the assessment and gradation. The software tools available can be used which not only gives the accurate analysis of the results obtained by the students after performing the experiment but also student himself can verify his/her results of experiments. This reduces the time required for evaluation of an experiment; rather teacher can now concentrate more on setting the challenging assignments to the students. Through this platform we aim to impart knowledge about innovative assessment methods to the participants particularly in the domain of VLSI design, embedded systems and DTSP.

Resource persons:

1. Dr. Prachi Gharpure, Principal, S.P.I.T.
2. Dr. Surendra Rathod, HOD ETRX, S.P.I.T.
3. Dr. D. R. Kalbande, HOD COMP, S.P.I.T.
4. Dr. D. V. Bhoir, HOD ETRX, CRCE
5. Dr. Jonathan Joshi, CEO Eduvance
6. Mr. Ganesh Gore, CTO Eduvance

Schedule:

DAY-1
1. Implementation of outcome based eduation-I
2. Implementation of outcome based eduation-II
3. Self Learning Session on Embbeded System
DAY-2
4.Articulation of PO- CO
5.Evaluation of PO-CO
6. Self Learning Session on FPGA Programming
DAY-3
7.Innavative practices in teaching & learning
8. Innavative practices in teaching & learning
9. Innovative method of assessment-I : VLSI Design
DAY-4
10. Innovative method of assessment-II: Embbeded Systems
11. Innovative method of assessment-III: DTSP
DAY-5
12. Discussion on SAR