

Two-day training on

Mentor Graphics VLSI Tools

12-13 January 2012

To,

Department of Electronics / Electronics and
Telecommunication Engineering,
Sardar Patel Institute of Technology,
Munshi Nagar, Andheri (W),
Mumbai 400 058
Phone: 26707440/26708520 Extn. 321/ 330

From,

Organizing Committee:

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Vice Principal: Dr. Y. S. Rao

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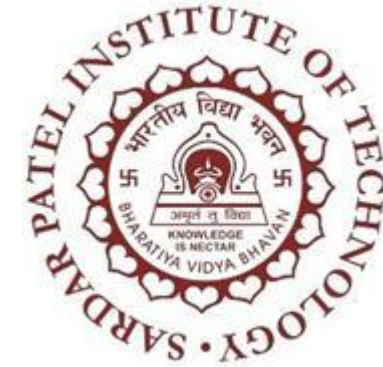
**Sardar Patel Institute of Technology
Bhavan's Campus, Munshi Nagar,
Andheri (W), Mumbai 400 058**

Tel: 91-22-2670 8520, 26707440, 2628 7250

Fax No.: 91-22-26701422

Bus from Andheri (W): 249/250/254/257/259

Bharatiya Vidya Bhavan's



**Sardar Patel Institute of Technology
in association with
Trident Techlabs Pvt. Ltd., Pune**

PRESENTS

Two-day training

on

Mentor Graphics VLSI Tools

12-13 January 2012

Organized by

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Telecommunication Engineering,
Sardar Patel Institute of Technology,
Munshi Nagar, Andheri (W),
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www.spit.ac.in

About us

In 1957, the Bharatiya Vidya Bhavan conceived the idea of establishing an engineering college in Mumbai. It was on the 19th August 1962 that there was a huge gathering at the Bhavan's Campus in Andheri to inaugurate Sardar Patel College of Engineering (SPCE). In 1995 Self Financed Engineering Course were added to it and it functioned as SPCE (Unaided-wing) conducting Electronics Engineering, Computer Engineering and Information Technology courses and Masters course in Electronics since 2005 till 2008. These courses have earned a great reputation in the field of engineering education, as well as industry. Bharatiya Vidya Bhavan's Sardar Patel College of Engineering, Unaided Wing from year 2005-2006 was established in its new building under the name and style of Bharatiya Vidya Bhavan's Sardar Patel Institute of Technology and is affiliated to Mumbai University. Subsequently Electronics and Telecommunication courses were started at graduate and post graduate level in year 2006 and 2010 respectively.

About the Training

It has become important for the educators, practicing engineers and the students, to continuously update their knowledge and skills in VLSI circuit and layout design. To verify theoretical concepts it is necessary to know the simulation tool very well. To achieve this goal, S.P.I.T. has invited engineers from Trident Techlabs to impart two day training on mentor graphics tools. Trident Techlabs Pvt. Ltd. is a leading EDA tools provider and authorized partner for M/s Mentor Graphics Inc., USA. S.P.I.T. has 25 user licenses for mentor graphics tools on which actual hands-on sessions will be conducted.

Who should attend:

Faculties, Research Scholars, UG & PG Students and Industry Professionals.

Topics to be Covered:

VLSI Design Methodologies
Spice Level Simulation Using "Eldo"
Physical Layout Using "IC Station"
Physical Verification Using "Calibre"

Resource Persons:

1. Dr. S. S. Rathod (S.P.I.T.)
2. Experts from Trident Techlabs Bangalore and Pune

Schedule:

12 Jan 2012

Demo/Theory: 10.00 am to 1.00 pm
Lunch: 1.00 pm to 2.00 pm
Hands-on Practical: 2.00 pm to 5.00 pm

13 Jan 2012

Demo/Theory: 10.00 am to 1.00 pm
Lunch: 1.00 pm to 2.00 pm
Hands-on Practical: 2.00 pm to 5.00 pm

Venue:

VLSI Lab, 310, 3rd Floor, S.P.I.T.

Course Fees:

Participants from Academic Institutes: Rs. 3000/--
PG Students (College ID Compulsory): Rs. 2000 /-
Participants from Industry: Rs. 4000 /-

Registration:

Cheque or DD drawn in the name of "ESA-SPIT" payable at Mumbai should reach on or before 10 Jan 2012 along with application form.

Two-Day training on Mentor Graphics VLSI Tools

12-13 January 2012

Name: _____

Designation: _____

Qualification: _____

Experience: _____

Institution: _____

Address: _____

Email: _____

Tel: (O) _____ (Extn.) _____

(M) _____ (R) _____

Payment by Cash / Cheque / DD:

Chq. /DD No: _____ Dated: _____

Bank: _____

Amount Rs.: _____

(Cheque / DD, should be in the name of "ESA-SPIT", payable at Mumbai)

Signature of the participant