


1	Name of Teaching Staff :	Surendra Singh Rathod		
2	Designation :	Assistant Professor		
3	Department :	Electronics and Telecommunication		
4	Date of Joining the Institution :	1 st Oct 1999		
5	Qualification with Class / Grade :	UG	PG	Ph.D.
		First	Distinction	Pursuing at IIT Roorkee
6	Total Experience in years :	Teaching	Industry	Research
		12 Years	nil	02 years
7	Papers Published:	National		International
		Nil		06
8	Papers Presented in Conferences :	National		International
		18		24
9	Phd Guide? Give field and University :	Field:Nil		University:Nil
10	PhDs / Projects Guided :	Ph.Ds:Nil		Projects at Masters level:Nil
11	Books Published / IPRs / Patents :	Nil		
12	Professional Memberships :	IEEE, ISTE, VSI, ISNT		
13	Consultancy Activities :	Nil		

14	Awards :	<p>1. Received 'Outstanding Achievement Award' for year 2007 by Energy Society of India and College of Engineering Pondicherry by his Excellency, Government of Pondicherry.</p> <p>2) Won Best Paper Award for the Paper Titled "VLSI Implementation of a Viterbi Decoder" in the national conference held at Government College of Engineering, Aurangabad on 23rd & 24th Jan 2006.</p> <p>3) Won Best Paper Award for the Paper Titled "Design and Simulation of PC to SRAM Interface for Reconfigurable Processors" in the national conference held at MIT, Manipal on 11th & 12th Nov 2005.</p> <p>4) Prize winner in Project/Competition by Institution of Engineers(India) held at Nagpur on 16th and 17th March 1997.</p>
15	Grants fetched :	Nil
16	Interaction with Professional Institutions:	Nil
17	Subjects taught till today	<p>1. VLSI Design</p> <p>2. Basics of VLSI</p> <p>3. Microprocessor</p> <p>4. Analog and Digital Integrated Circuits</p>

18. Conference / Seminar Attended / Paper Published		
International		
18.1	Published	24
18.2	Attended	Nil
National		
18.3	Published	18
18.4	Attended	Nil
18.5	Journal Papers	06 (Please refer attachment)
18.6	STTP	02
18.7	CEP	09
18.8	Industrial Training / Workshop	Nil
18.9	M.E. / M.Tech.	Nil
18.10	Ph.D.	Nil

Few Recent Published/Accepted Publications

International Journals:

1. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Robust Double Gate FinFET based Sense Amplifier Design Using Independent Gate Control," *Journal of Low Power Electronics*, vol. 6, no. 4, pp. 533-544, Dec. 2010.
2. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "A Proposed DG-FinFET based SRAM cell Design with RADHARD capabilities," *Microelectronics Reliability*, vol. 50, no. 8, pp. 1181-1188, Aug. 2010.
3. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Electrical Performance Study of 25 nm Ω -FinFET under the Influence of Gamma Radiation: A 3D Simulation," *Microelectronics Journal*, vol. 42, no. 1, pp. 165-172, Jan. 2010.
4. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Low Noise, Process Variation Tolerant DG-FinFET based Sense Amplifier," *Microelectronics Reliability* (Accepted: In-Press).
5. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Alpha Particle Induced Effects in PD-SOI Device: With and Without Body Contact," *IET Circuits, Devices and Systems*, (Accepted: In-Press).
6. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Study of Quantum and Classical Transport in 25nm Omega FinFET under Gamma Radiation: 3D Simulation Study," *Journal of Active and Passive Electronic Devices*. (Accepted: In-Press).

International Conferences:

1. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Analytical Modeling for Subthreshold Leakage Current in Irradiated FinFET Device," *Int. Conf. on Communication, Computers and Devices (ICCCD)*, IIT Kharagpur, India, pp. 1-4, 10th -12th Dec. 2010.
2. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Effect of Border Traps on Electron Mobility of Nanoscale MOS Devices," *IEEE Int. Symp. on Electronic System Design (ISED)*, Bhubaneswar, India, pp. 91-94, 20th -22nd Dec., 2010.
3. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Analytical Modeling for Estimation of Drain Current in Irradiated Nanoscale Double Gate FinFET Device," *14th IEEE VLSI Design and Test Symp. (VDAT 2010)*, Chandigarh, India, pp. -, 7th-9th Jul., 2010.

4. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Rad-Hard 32 nm FinFET based Inverters," *IEEE Int. India Conference (INDICON-2009)*, Gandhinagar, India, pp. 1-4, 18th-20th Dec., 2009. (Available on IEEE Xplore)
5. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Mixed Mode Simulation of Heavy Ion Impact on 3D SRAM cell," *IEEE 4th Int. Conf. on Computers and Devices for Communication (CODEC-09)*, Kolkata, India, pp. 1-4, 14th -16th Dec., 2009. (Available on IEEE Xplore)
6. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Effect of Gamma Radiation on 25nm Ω -FinFET: 3D Simulation Study," *IEEE XVth Int. Workshop on the Physics of Semiconductor Devices (IWPSD)*, New Delhi, India, pp. 1-4, 15th-19th Dec., 2009.
7. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "TCAD Modeling of SOI Structure for Reduction of Single Event Upset," *IEEE Regional Symp. on Micro and Nano Electronics (IEEE-RSM2009)*, Kota Bahru, Malaysia, pp. 135-140, 10th-12th Aug., 2009.
8. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Analysis of Single Event Upset for Biomedical Applications," *13th IEEE VLSI Design and Test Symp. (VDAT 2009)*, Bangalore, India, pp. 294-306, 8th-10th Jul., 2009.
9. S. S. Rathod, A. K. Saxena, and S. Dasgupta, "Investigation of Stack as a Low Power Design Technique for 6T-SRAM cell," *IEEE Region-10 Int. Conf. TENCON-2008*, Hyderabad, India, pp. 1-5, 18th-21st Nov., 2008. (Available on IEEE Xplore)